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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAJESH TIWARI, RUSSELL FIELDS,
SCOTT A. BODDICKER and ANDREW TAE KIM

Appeal 2007-1808
Application 10/663,948[1]
Technology Center 2800

Decided: January 23, 2008

Before HOWARD B. BLANKENSHIP, JAY P. LUCAS, and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1, 2, 4 and 9. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' invention relates to a method for forming a copper interconnect layer. A dielectric layer is formed over a semiconductor. A plurality of vias is formed in the dielectric layer to allow the subsequently

[1] Application filed September 16, 2003. The real party in interest is Texas Instruments Incorporated.

formed copper layer to contact an underlying copper layer. A trench is formed in the dielectric layer over the vias, with an edge that extends a minimum distance from the edge of the via closest to the trench. The trench and vias will be filled with copper to form a copper interconnect line. The minimum overhang of the copper line will reduce and/or eliminate copper delamination (Specification 3).

Claim 1 is exemplary:

> 1. A method for forming a copper interconnect layer, comprising:
> forming a first copper region over a semiconductor;
> forming a low K dielectric layer over said copper region;
> forming a plurality of vias in a first region of said low K dielectric layer;
> forming a trench with a first edge in said low K dielectric layer over said plurality of vias wherein said trench extends a minimum length of 0.2 μm beyond the edge α of a via closest to the first edge of said trench; and
> filling said trench and said plurality of vias with copper.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Shimizu	6,433,432 B2	Aug. 13, 2002
Watanabe	2003/0227089 A1	Dec. 11, 2003

Claims 1, 2, 4 and 9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Shimizu in view of Watanabe.

Appellants contend that the Examiner erred in his rejections because neither Shimizu nor Watanabe teach requiring a minimum overhang length between the trench edge and the closest via edge (Br. 3). The Examiner

contends that the claims are properly rejected because Shimizu teaches a trench with an overhang, and Watanabe teaches an overhang length at least as long as the minimum recited in the claims, rendering the invention obvious.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The principal issue in the appeal before us is whether the Examiner erred in holding that the person having ordinary skill in the art would have found it obvious to modify Shimizu in accordance with the teachings of Watanabe in order to produce a semiconductor structure including a trench with an overhang having the dimensions claimed.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. Appellants invented a semiconductor structure including a plurality of vias in a dielectric layer to allow a subsequently formed copper layer to contact an underlying copper layer. A trench is formed in the dielectric layer over the plurality of vias, with an edge that extends past the edge of a via closest to the edge of the trench (Specification 3).

2. The trench and vias are filled with copper to form a copper interconnect line. The overhang of the copper line will reduce or eliminate copper delamination (Specification 3).

Shimizu

3. Shimizu teaches a semiconductor device capable of maintaining good connection between a metal film buried in a trench of a fluorine-containing insulating film and another metal film connected to such metal film (col. 2, ll. 19-23).

4. Shimizu recognizes the problem of copper delamination ("peeling off") of the "plugs" of copper filling the vias from the upper surface of the wiring. Shimizu relies on adhesion between the copper wiring and the overlying plugs and film in order to prevent such "peeling-off" (Br. 5-6). Sputter is performed to remove fluorine from the surface of the copper wiring, and shoulder formation is merely an unintended by-product thereof (Br. 6; col. 2, ll. 1-16 and 32-43).

5. Shimizu teaches forming a first copper region over a semiconductor substrate (col. 4, ll. 55-57); forming a low K dielectric layer over the copper region (col. 5, ll. 27-30 and col. 1, ll. 16-21); forming a plurality of vias (Fig. 3J, 12a) in a first region of the low K dielectric layer; forming a trench (Fig. 3J, 16) with a first edge in the low K dielectric layer over the plurality of vias, the trench extending (some) minimum length beyond the edge of a via (Fig. 3J, overhang by pad trench 12b); and filling the trench and the plurality of vias with copper (col. 5, ll. 61-63).

Watanabe

6. Watanabe teaches a semiconductor device which can prevent cracks and suitably intercept entry of moisture, and a method of manufacturing the same (para. [0023]).

7. In one embodiment, an upper layer wiring pattern and via patterns are formed via the dual damascene method (para. [0172]).

8. Watanabe teaches a trench-and-via structure as claimed by Appellants, with the trench extending beyond the edge of the "last" via (Fig. 24C; para. [0172],[0175]).

9. The trench overhang extends 4.25 μm beyond the edge of the via, assuming there are three vias as illustrated in Figs. 24B and 24C (Ans. 6; Watanabe para. [0175]).

10. The written description in Watanabe discloses sixteen vias, rather than the three illustrated in the Figures (para. [0175]).

11. Watanabe's sample dimensions show the width of a via as 0.3 μm, a via pitch (defined as one via plus the spacing between vias) as 0.6 μm, and the full width of the wiring pattern as 10 μm (para. [0175]).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR Int'l. Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (*citing In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Only if this initial burden is met does the burden

of coming forward with evidence or argument shift to the Appellant. *Piasecki*, 745 F.2d at 1472. Thus, the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion.

ANALYSIS

Appellants argue that the Examiner erred in rejecting claims 1, 2, 4, and 9 because "Shimizu fails to require a *minimum* length between the trench edge and the closest via edge" and Watanabe fails to cure this deficiency (Br. 3)(emphasis in original). According to Appellants, Watanabe merely provides dimension examples of various wiring patterns and width patterns and does not teach or suggest a minimum length between a via edge and a trench edge (Br. 6).

Appellants further argue that Shimizu does not teach a trench overhang past the edge of a via *for the purpose of preventing delamination* (Br. 4; emphasis added). Shimizu relies on adhesion between the copper wiring and the overlying plugs and film in order to prevent such "peeling-off" (FF 4). Sputter is performed to remove fluorine from the surface of the copper wiring and the shoulder formation is merely an unintended by-product thereof (FF 4).

The Examiner acknowledges Appellants' position. Because Shimizu does not specify that the minimum length the trench extends is at least 0.2 μm, the Examiner directs Appellants to Watanabe, which teaches a trench and vias as claimed, with the trench extending beyond the edge of the "last" via (FF 8; Ans. 5). The Examiner calculates, based on the dimensions Watanabe provides (FF 11), that the trench extends 4.25 μm beyond the edge of the via (FF 9). We note that the Examiner's algebra is based on the circuit illustrated in Watanabe Figs. 24B and 24C, which show *three* vias (FF 9). The description of those figures recites that *sixteen* vias can be formed per one wiring pattern (FF 9). If there are sixteen vias rather than three, the trench overhang is calculated to be 0.35 μm^2 (FF 11).

Therefore, even if one assumes that Watanabe intended for the embodiment illustrated in Fig. 24 to have sixteen vias rather than just the three displayed, Watanabe still teaches that his trench extends a minimum of

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[2] P = pitch of the via patterns, i.e. the width of one via plus the area between one via and the next, disclosed as 0.6 μm (FF 11)

W(trench) = width of the entire wiring pattern, and also the full length of the trench, disclosed as 10 μm (FF 10)

W(vias) = width of via pattern, disclosed as 0.3 μm (FF 11)

A= 15P + W(vias)
= (15*0.6)+0.3
=9.3 μm

2L= W(trench)-A
=10 – 9.3
=0.7 μm

L = 0.7/2 = 0.35 μm

(i.e., *at least*) 0.2 μm (specifically, 0.35 μm) beyond the edge of the via closest to the first edge of the trench.

Like Shimizu, however, Watanabe does not teach preventing delamination as his *purpose* for forming a trench with an overhang. Watanabe is silent as to any purpose for the presence of his overhang structure.

As noted by the Examiner, Shimizu teaches forming a first copper region over a semiconductor substrate; forming a low K dielectric layer over the copper region; forming a plurality of vias in a first region of the low K dielectric layer; forming a trench with a first edge in the low K dielectric layer over the plurality of vias, the trench extending (some) minimum length beyond the edge of a via; and filling the trench and the plurality of vias with copper (FF 5; Ans. 3). Shimizu teaches a trench with an 'overhang' past the edge of the "last" via, but is silent as to the precise length of the overhang (see Fig. 3J, overhang by pad trench 12b).

The Examiner asserts that the combination would have been obvious because the trench overhang would, by its mere physical presence, have provided the benefit of preventing "the peeling-off of the plugs from the metal wiring," i.e., delamination (Ans. 6).

Appellants argue that Shimizu does not teach a trench overhang past the edge of a via for the purpose of preventing delamination, but rather that Shimizu teaches other manufacturing steps to prevent such "peeling-off" (Br. 4; see FF 4).

We agree with Appellants' position. Shimizu does not teach that his overhang is provided for the purpose of preventing delamination. Watanabe

(incidentally, it seems) teaches a trench with an overhang, but also fails to teach that his overhang is provided, or would serve, for the purpose of preventing delamination. The Examiner's assertion that "such minimum length would provide the same effects of preventing the peeling-off of plugs from the metal wiring" (Ans. 6) lacks support in Shimizu or Watanabe. It appears that the Examiner means to imply that such prevention would be inherent; however, the Examiner did not explain his basis for holding that prevention of delamination would necessarily be present given an overhang of the appropriate "minimum length."

We agree with Appellants that the person of ordinary skill in the art would not have found it obvious to modify Shimizu to include an overhang as taught by Watanabe, because neither reference teaches the desirability of making the combination, and because neither reference teaches that providing a trench with an overhang would address the problem of delamination.

As a result, we reverse the rejection of claims 1, 2, 4, and 9.

CONCLUSION OF LAW

We conclude that Appellants have shown that the Examiner erred in rejecting claims 1, 2, 4, and 9. On the record before us, claims 1, 2, 4, and 9 have not been shown to be unpatentable.

DECISION

The Examiner's rejection of claims 1, 2, 4 and 9 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED

tdl/gvw

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